A 200GHz Downconverter in 90nm CMOS

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***Abstract*— A 200 GHz downconverter in 90 nm standard CMOS is presented with a measured positive conversion gain of $+6.6$ dB and an IF bandwidth of 3 GHz for an LO power of -14.9 dBm. The conversion gain has a flatness of ± 1.5 dB in an LO frequency range of 26 GHz. The IIP$_3$ is -5.4 dBm. BPSK and QPSK data downconversion are demonstrated with a data rate of over 4 Gbit/s.**

I. Introduction

As CMOS scaling continues, new opportunities arise for electronic integrated circuits working at ever higher frequencies. The millimeter wave frequency range, including the G-band from 140 to 220 GHz, allows applications such as high speed short range communication, imaging and radar. In this paper, the design and measurements of a 200 GHz downconverter are discussed. The LO frequency (f_{LO}) of the mixer is 200 GHz, which is well above the f_T (144 GHz) of the used technology. The IF output has a bandwidth of several GHz To the author's knowledge, this is the first integrated down conversion mixer in CMOS above 200 GHz with demonstrated capability of Gbit/s data communication.

II. Circuit design and implementation

Fig. 1 shows the architecture of the complete downconverter chip. The circuit can be divided into two parts, according to their operating frequency: the RF part and the IF part. The former consists of the RF and LO transformers and the four mixing transistors. The latter comprises a transimpedance amplifier (TIA), voltage gain stage and voltage buffer.
The four mixing transistors, together with the TIA, form an active MOSFET-C mixer. Because of the high frequency, the MOSFETs can not be used as switches anymore, but instead they are used as variable resistors.

A. Design of the mixing transistors

The four NMOS mixing transistors perform the actual mixing operation of the 200 GHz LO and RF signals, based on the MOSFET-C mixer principle [1]. They are biased in the linear region ($V_{DS} = 0$) and are arranged as a double balanced structure. The LO is applied to the drains and the RF is applied to the gates. The gate voltage varies the MOSFET's channel resistance, generating a current which is proportional to the product of the LO and the RF voltages, as can be seen from the well known equation for a MOSFET in the linear region:

$$i_{DS} = \mu C_{ox} \frac{W}{L}[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}] \qquad (1)$$

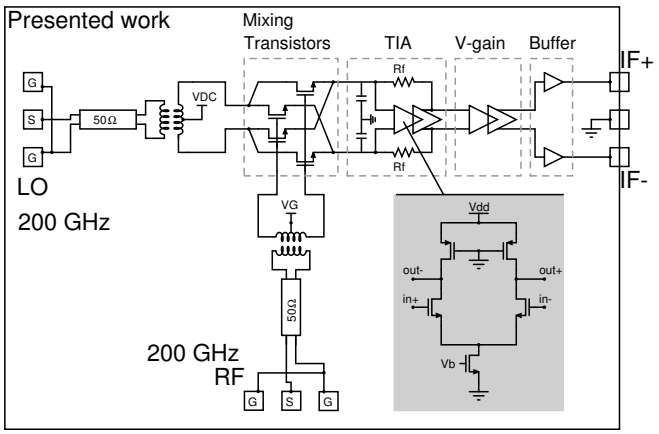

Fig. 1. Circuit diagram of the complete 200GHz downconverter chip

The double balanced structure cancels unwanted mixing products, while the input capacitance of the TIA (explicitly shown in figure 1) filters out high frequencies so that only the IF signal remains.
The NMOS mixing transistors are laid out in a triple-well structure as to allow the bulk voltage to be set independently from the IF part of the circuit. The bulk voltage is chosen equal to the DC voltage on the drains and sources of the mixing transistors in order to eliminate the bulk effect. This DC voltage is at the same time the bias voltage on the gates of the input transistors of the TIA.
The gate length of the mixing transistors is minimal: $L = 90$ nm and the finger width: $W_F = 1$ µm. The number of fingers is 6. This determines the impedances presented to the RF and LO transformers to guarantee maximum power transfer to the transistors. The gate-source voltage is set to $V_{GS} = 0.38$ V for maximum conversion gain. Thus, the mixing transistors are optimized for maximum available IF power, given the available power of the RF and LO signals. Besides maximizing the conversion gain, this also minimizes the noise figure of the mixing transistors, whose contribution to the total noise figure is most important.

B. Design of the RF and LO transformers

The entire circuit is fully differential. Two on-chip 200 GHz transformers convert the unbalanced RF and LO signals to balanced signals for the mixing transistors. They match the impedance seen in the RF and LO connections of the mixing

transistors to $50\,\Omega$ at $200\,\mathrm{GHz}$ and they are also used for DC bias of the mixing transistors via the center tap of the secondary turn. This way, the gates of the input pair of the TIA are also biased, as mentioned before. Thanks to this approach, complicated bias circuits can be omitted. Both integrated baluns have a single turn in the primary and secondary coil. They are fabricated in the top metal, which is farthest away from the substrate and has a low resistivity. Their trace widths and diameters are optimized toward impedance matching and minimum loss using Momentum.

C. The IF part

The function of the TIA is to convert the IF current from the mixing transistors into a voltage. The TIA is designed as a cascade of differential voltage amplifiers, with feedback resistors R_f, see Fig. 1. Each voltage amplifier has finite gain and bandwidth. Cascading them increases the gain but decreases the bandwidth [2]. The feedback resistors determine the transimpedance and the bandwidth of the TIA. Considering these influences, two voltage amplifiers are cascaded and the feedback resistors are chosen to be $R_f = 1\mathrm{k}\Omega$. The voltage gain stage is again a cascade of two of the same voltage amplifiers. The voltage buffers are designed to drive a $50\,\Omega$ load.

D. Layout

To determine the correct impedances seen at the gates and drains of the mixing transistors and to minimize resistive losses, parasitic extraction is done for the mixing transistors and Momentum simulations are performed for all the surrounding interconnections.
In the IF part, parasitic extraction is done for the TIA, voltage amplifiers and source followers, in order to accurately simulate the performance.
In the chip micrograph (Fig. 9), the transformers can be clearly distinguished. In between them are the mixing transistors and above them is the IF part.

III. Measurement Results

The design has been fabricated in a $90\,\mathrm{nm}$ standard CMOS process. The chip is mounted on an FR-4 PCB for measurements. The $200\,\mathrm{GHz}$ LO and RF signals are generated by millimeterwave source modules and applied to the chip through G-band waveguide probes. The IF output is brought off-chip through bondwires. The measurement setup on the probe station is shown in Fig. 2.

Applying the LO with a frequency of $f_{\mathrm{LO}} = 200\,\mathrm{GHz}$ and a power of $P_{\mathrm{LO}} = -14.9\,\mathrm{dBm}$ and the RF with a frequency of $f_{\mathrm{RF}} = 200.5\,\mathrm{GHz}$ and a power of $P_{\mathrm{RF}} = -16.6\,\mathrm{dBm}$ results in a $500\,\mathrm{MHz}$ IF with a power of $P_{\mathrm{IF}} = -10.0\,\mathrm{dBm}$. The measured conversion gain is $+6.6\,\mathrm{dB}$. As can be seen in Fig. 3, the conversion gain varies linearly with the applied LO power, as is expected for this type of circuit.
Linearity is measured for $P_{\mathrm{LO}} = -14.9\,\mathrm{dBm}$, by varying the RF input power and tracking the first harmonic at $500\,\mathrm{MHz}$ (P_{IF}) and the third harmonic at $1.5\,\mathrm{GHz}$ (P_3). Simulations

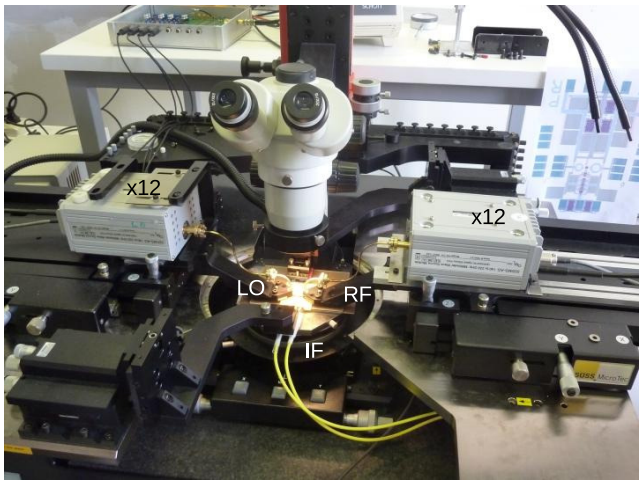

Fig. 2. Photograph of the measurement setup for a 200 GHz downconverter IC, showing the G-band source modules. Signals are applied through probes.

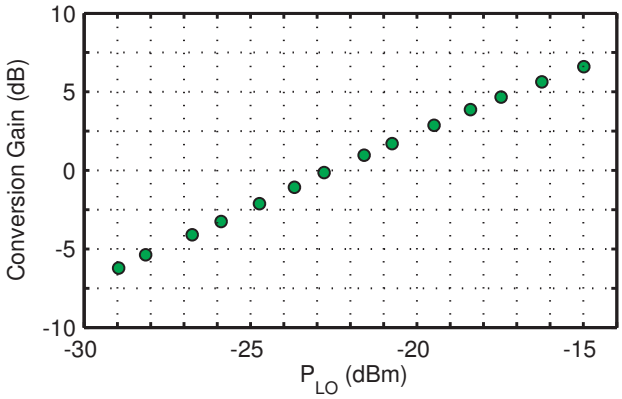

Fig. 3. Measured conversion gain versus P_{LO}.

indicate that the linearity of the complete chip is limited by the IF part only and not by the $200\,\mathrm{GHz}$ mixing transistors. Although a true two-tone test could not be performed, the IP_3 can be calculated from the theoretical link between the third order intermodulation product (IM_3) and P_3: $\mathrm{IM}_3 = P_3 + 9.54\,\mathrm{dB}$. As a result, the input third order intermodulation intercept point is: $\mathrm{IIP}_3 = -5.4\,\mathrm{dBm}$. This corresponds very well to the simulations, as shown in Fig. 4.

The IF output bandwidth is measured by changing f_{RF} while keeping f_{LO} fixed at $200\,\mathrm{GHz}$. As can be seen in Fig. 5, the IF bandwidth is $3\,\mathrm{GHz}$. This is limited by the IF gain stages but also by the bondwires and the FR-4 PCB.
The conversion gain deviates less than $\pm 1.5\,\mathrm{dB}$ within an LO and RF frequency range of $26\,\mathrm{GHz}$: from $186\,\mathrm{to}\,212\,\mathrm{GHz}$. This is measured by changing f_{RF} and f_{LO} simultaneously while keeping f_{IF} fixed at $500\,\mathrm{MHz}$. This downconverter can be used for carrier frequencies anywhere between $186\,\mathrm{and}\,212\,\mathrm{GHz}$. The reason is that the transformers match the mixing transistors with $50\,\Omega$ in a very wide band.
The output noise measurements and simulations are shown

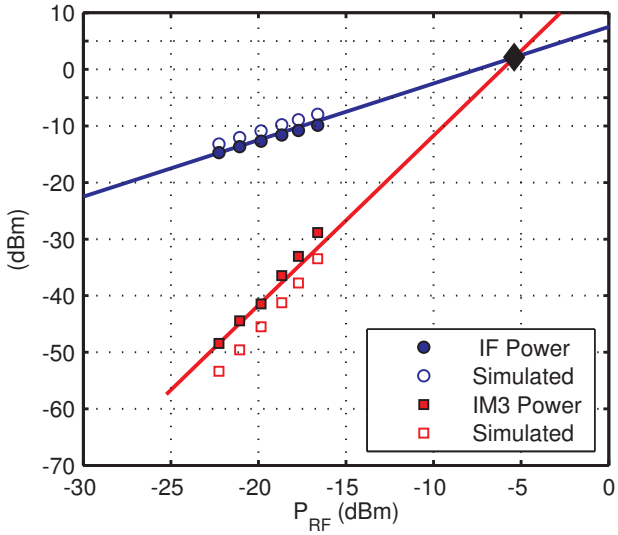

Fig. 4. Measured and simulated P_{IF} and IM_3 versus P_{RF}.

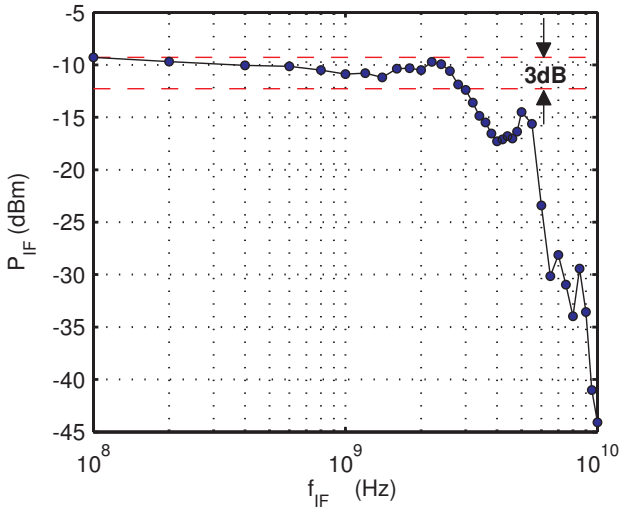

Fig. 5. Measured IF bandwidth is 3 GHz.

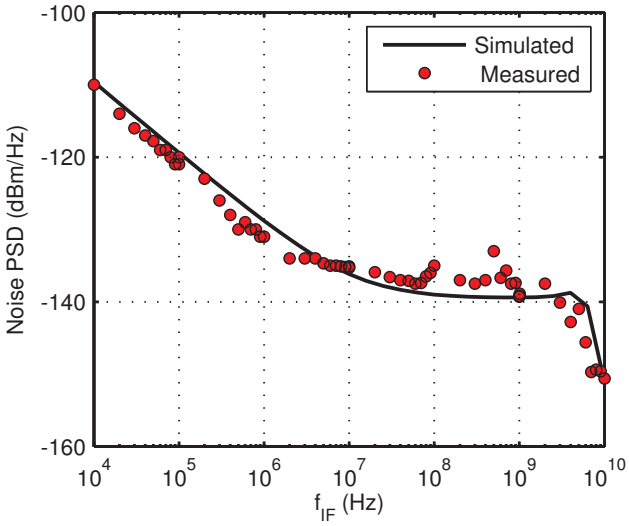

Fig. 6. Measured and simulated output noise density. 1/f noise corner around 10 MHz, average noise level in a band from 10 kHz to 3 GHz: -137.5 dBm/Hz

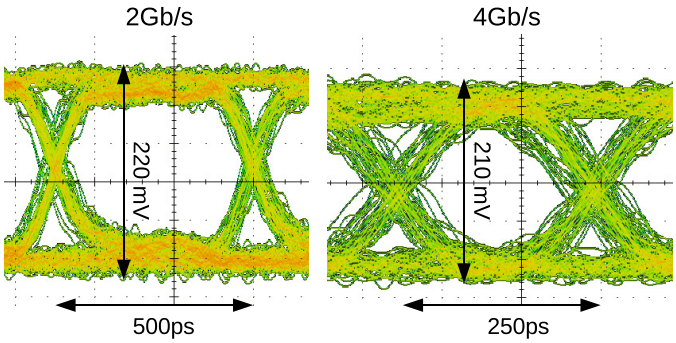

Fig. 7. Measured eye diagrams for BPSK with data rates of 2 Gbit/s (a) and 4 Gbit/s (b), downconverted to baseband.

in Fig. 6. The average noise level in a band from 10 kHz to 3 GHz is -137.5 dBm/Hz. The 1/f noise corner frequency is around 10 MHz. Compared to the 3 GHz bandwidth, the 1/f noise can be neglected. From the integrated noise, the noise figure can be calculated:

$$\mathrm{NF} = 10 \times \log\left(\frac{N_o}{GkTB}\right) = 29.9 \text{ dB} \qquad (2)$$

Where N_o is the integrated output noise power in the band, calculated from the measured data. G is the conversion gain and kTB is the available input noise power. This is a single sideband (SSB) noise figure since it assumes a signal on one side of the LO frequency only.

As a demonstration of the IC's high-speed data communication capability at millimeterwave frequencies, a test setup was conceived to generate 200 GHz BPSK and QPSK modulated signals to apply to the RF input. The millimeter wave source module multiplies any phase or frequency information at its input with a factor of twelve. Therefore, signals are first generated that, when applied to the source module's input, give the desired BPSK or QPSK signals at the output. By choosing the LO frequency equal to the carrier frequency of the modulated signals, the presented IC mixes the signal to baseband. The output of the downconverter can be visualized on an oscilloscope in the form of eye diagrams. In Fig. 7, eye diagrams for 2 Gbit/s and 4 Gbit/s BPSK are shown.

Fig. 8 shows the measured constellation diagrams for BPSK and QPSK signals downconverted to different IF frequencies for various data rates.

It is thus shown that the presented downconverter IC is capable of achieving high data rates at G-band frequencies. It should be noted that the speed is limited by the IF part and the FR-4 PCB and not by the 200 GHz mixing transistors. The speed can be easily enhanced by optimizing the IF blocks.

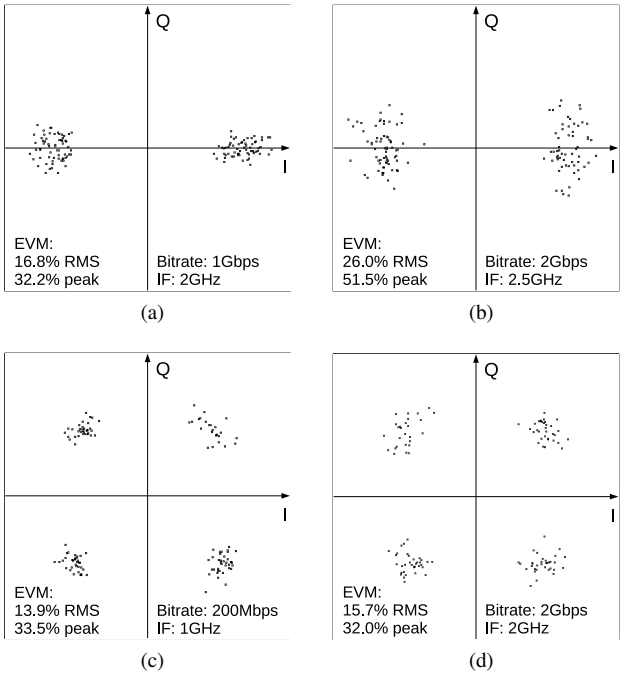

Fig. 8. Measured downconverted constellation diagrams for BPSK with data rates of 1 Gbit/s (a) and 2 Gbit/s (b) and QPSK with data rates of 200 Mbit/s (c) and 2 Gbit/s (d), at different IF frequencies.

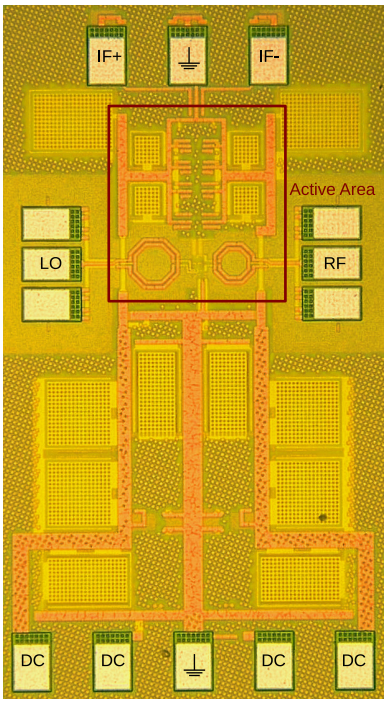

Fig. 9. Chip micrograph with indication of the active area.

The circuit draws 53 mA from a 1.2 V supply voltage. This power is consumed in the TIA, the voltage gain stage and the buffer stage.

A die photograph is shown in Fig. 9. The chip has an area of 0.375 mm^2, this includes the whole circuit, bond pads and probe pads. The active area as indicated in Fig. 9 is only 0.04 mm.

IV. Conclusion

In table I, the performance of this chip is summarized and compared to other work. The presented work is the only downconverter at these high frequencies with both positive conversion gain and considerable IF bandwidth. Moreover, the required LO power is relatively low, which is an important consideration in this frequency region. To the author's knowledge, this circuit is also the only one capable of downconverting modulated signals with high data rates, at carrier frequencies above f_{max}.

TABLE I

Performance summary and comparison to other work

Reference	[3]	[4]	[5]	This work
Process	0.1 µm GaAs mHEMT	65 nm CMOS	0.25 µm CMOS	90 nm CMOS
RF (GHz)	220	102	650	200
IF (MHz)	2000	2000	0 to 1.6	0 to 3000
Conv. Gain (dB)	-12	-4	-	+6.6
IIP_3 (dBm)	-	-	-	-5.4
NF (dB)	8.4 DSB	22	68 SSB	29.9 SSB
P_{LO}(dBm)	-	+1	-32.5	-14.9
P_{DC}(mW)	-	-	-	63.3
Area (mm^2)	3	-	-	0.375
Data rate (Gbit/s)	-	-	-	> 4

Acknowledgment

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